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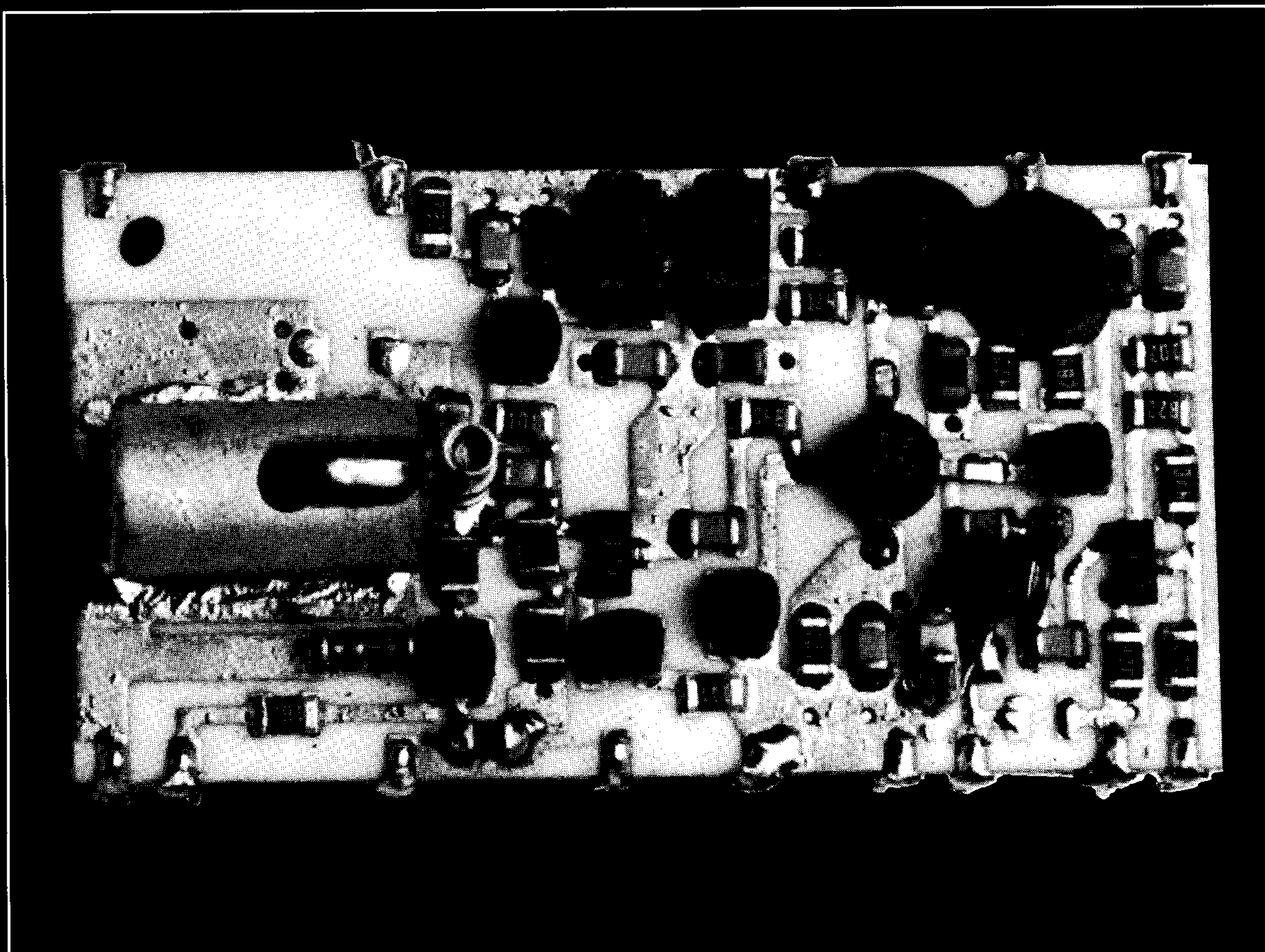

Low Phase Noise—How to Achieve It

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Designing Low-Phase-Noise Oscillators

Find an oscillator design that ensures low phase noise using modern computer programs.

by Dr. Ulrich L. Rohde, KA2WEU

As the other characteristics of communication equipment improve with technology, the stability of the signals generated in systems becomes increasingly important. Most often, we use oscillators to generate these signals. Thus it becomes important to determine how best to ensure stability in oscillator designs. This is particularly true of voltage-controlled oscillators (VCO), which typically use relatively low-Q resonators (compared to crystal oscillators, for example).

Oscillator performance can be considered to be composed of both short-term and long-term stability. Short-term stability is what we refer to as *phase noise*, and has been described in detail previously.[1] In this article, we will investigate means of designing oscillators that achieve low-phase-noise performance. The trend in modern design is toward low power and small size, driven in part by the use of hand-held, battery operated equipment. Power consumption influences noise performance because the ultimate signal-to-noise ratio at frequencies far removed from the oscillator frequency is determined by the output power—and thus by the power consumed. Physical size is a limiting factor on the Q of the resonator, which is partly responsible for determining close-in phase noise; larger resonators can achieve higher Qs. This article details methods of optimizing oscillator designs based on these principles. We also briefly look at the advantages of using ceramic resonators at UHF.

[1]Notes appear on page 12.

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Oscillator Noise

The SSB phase noise of an oscillator is well described by the Leeson model and its enhancements. Leading engineers such as M. Driscoll of Westinghouse and Tom Parker of Raytheon have expanded the model to include the flicker-noise component of even passive components.[2,3] The enhanced Leeson equation, as proposed by Parker and others, is shown in Fig 1.

Numerous circuits have been developed to implement oscillators. Fig 2 shows the most common RF oscillator circuit configurations. These circuits have various advantages and disadvantages, depending on the frequency of operation and the resonator type. For circuits in the 400 to 2000-MHz range, modern oscillators tend to use transmission-line resonators and capacitive feedback of the Colpitts or Clapp type. At these frequencies, bipo-

$$S_\phi(f_m) = \left[\alpha_R F_o^{\,4} + \alpha_E\left(F_o/(2Q_L)\right)^2\right]/f_m^{\,3}$$
$$+\left[\left(2GFKT/P_o\right)\left(F_o/(2Q_L)\right)^2\right]/f_m^{\,2}$$
$$+\left(2\alpha_R Q_L F_o^{\,3}\right)/f_m^{\,2}$$
$$+\alpha_E/f_m + 2GFKT/P_o$$

Fig 1—The Leeson equation for oscillator phase noise. *G* is the compressed power gain of the loop amplifier, *F* is the noise factor of the loop amplifier, *K* is Boltzmann's constant, *T* is the temperature in Kelvins, P_o is the carrier output power, in watts, at the output of the loop amplifier, F_o is the carrier frequency in Hz, f_m is the carier offset frequency in Hz, Q_L is the loaded Q of the resonator in the feedback loop, and α_R and α_E are the flicker noise constants for the resonator and loop amplifier, respectively.

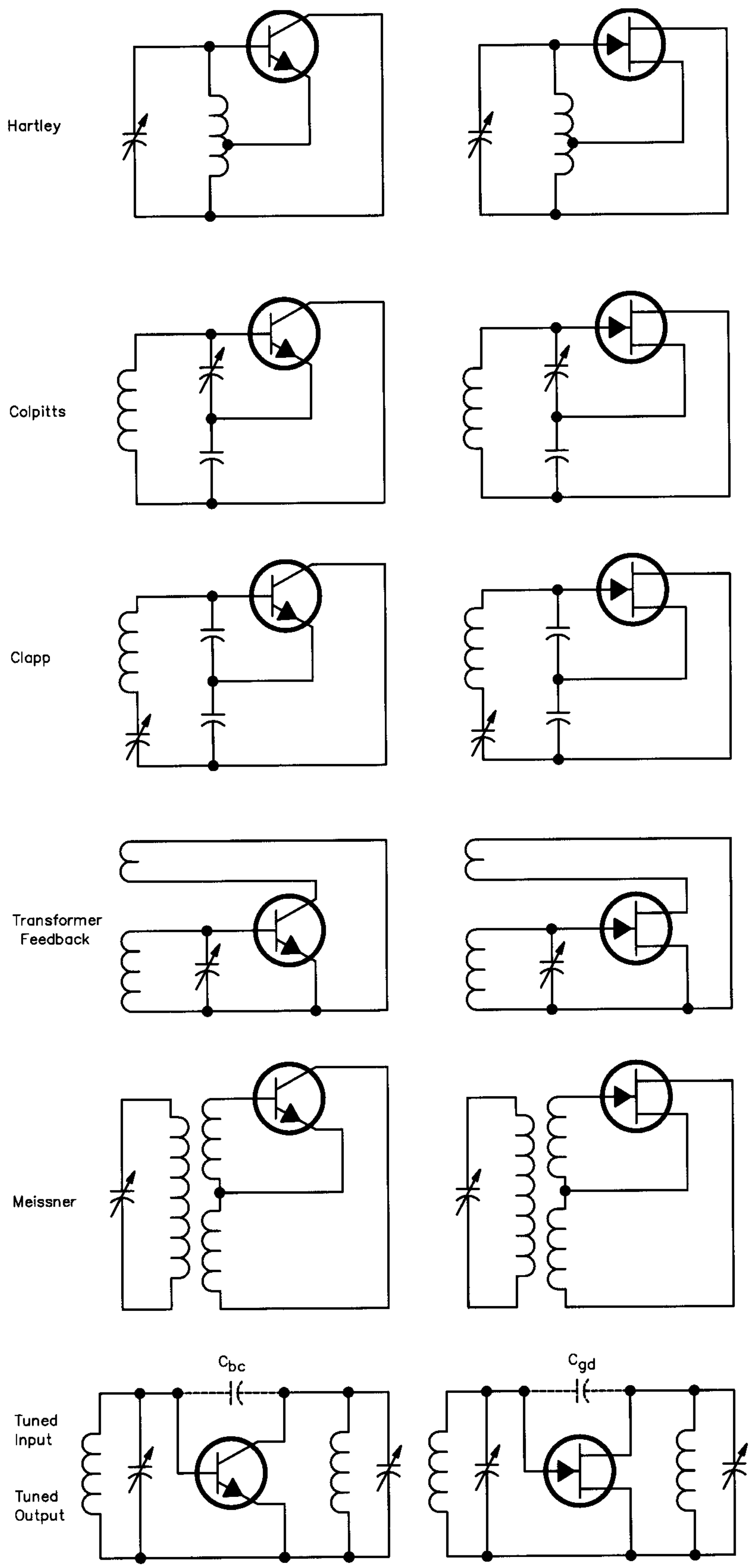


Fig 2—Common oscillator circuits for bipolar transistors and FETs.

lar transistors are generally used since few FETs have sufficient gain-bandwidth product for use in UHF oscillator circuits.

Requirements for Low-Noise Oscillators

The key elements that determine the phase noise of an oscillator are:

- the transistor's flicker-noise corner frequency, which depends on the device current;
- the loaded Q of the resonator, which depends on the coupling between the resonator and the transistor; and
- the ultimate signal-to-noise ratio, which depends on the RF output power of the oscillator and its large-signal noise figure.

Of these, the first two can be considered using linear analysis of the circuit. But the active device's large-signal operation requires nonlinear analysis techniques, without which we can make only educated approximations of the ultimate signal-to-noise ratio.

The Linear Approach

The design goal of the linear approach is to achieve the maximum loaded Q of the resonator and to keep the bias (dc) device current to a minimum. A high Q helps restrict noise components to frequencies close to the frequency of oscillation, minimizing phase noise as we move away from that frequency. The requirement for minimum bias exists because the flicker, or 1/*f*, noise of the device is highly dependent on the current. Table 1 shows the flicker-noise corner frequency versus collector current for a typical bipolar transistor. JFETs have much less flicker noise than bipolar transistors, while GaAs FETs have more.

Oscillator Operation

At start-up, the oscillator's open-loop gain must be sufficient to begin

Table 1—Flicker Corner Frequency vs Collector Current for a Typical Bipolar Transistor (from Note 6)

I_c (mA)	F_c (kHz)
0.25	1
0.5	2.74
1	4.3
2	6.27
5	9.3

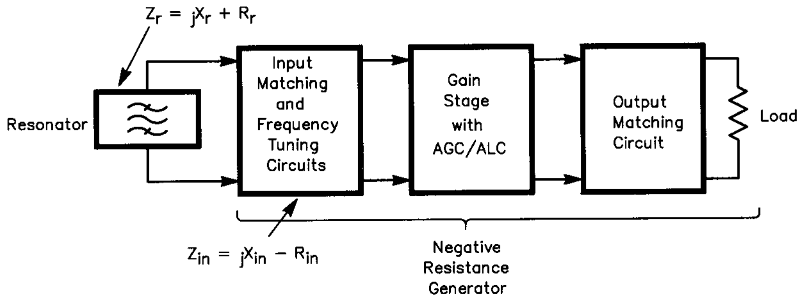


Fig 3—An oscillator viewed as a resonator and a negative resistance generator. At start-up, the resonator and oscillator reactances must be equal in value and opposite in sign, while the sum of the resonator and oscillator resistances must be less than 0. For sustained oscillation, the sum of the resistances must not become positive.

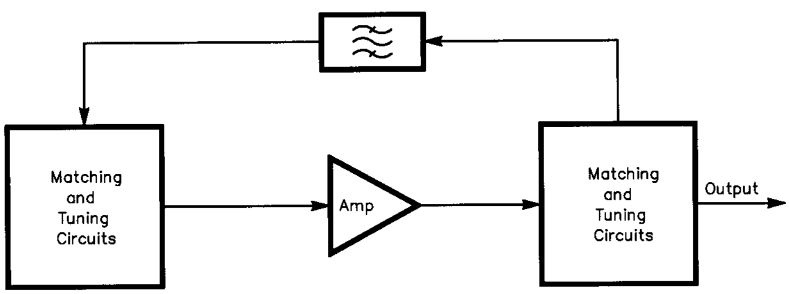
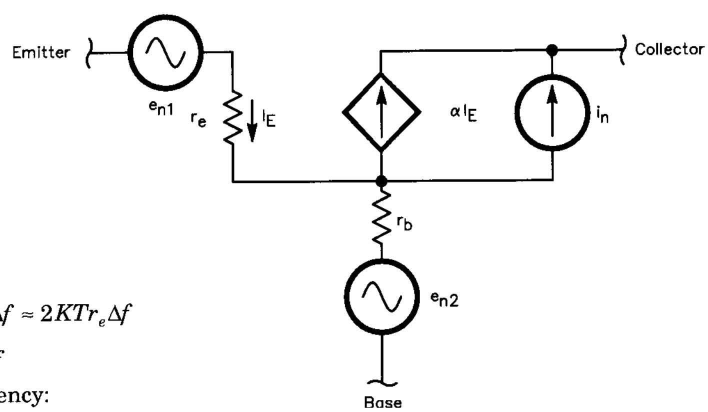


Fig 4—An oscillator viewed as a feed-forward amplifier with positive feedback through the resonator. Start-up of oscillation requires that the gain of the amplifier exceed the loss of the resonator and that the total phase shift through the amplifier and resonator be a multiple of 360°. To sustain oscillation, the phase shift must remain the same and the amplifier gain must be equal to or greater than the resonator loss.



$$\bar{e}^2_{n1} \approx 2qI_E{r_e}^2\Delta f \approx 2KTr_e\Delta f$$

$$\bar{e}^2_{n2} \approx 4KTr_b\Delta f$$

At high frequency:

$$\bar{i}^2_n \approx 2_q\left[\alpha_F I_E \frac{1-\alpha_F + f^2/{f_o}^2}{1+f^2/{f_o}^2} + I_{ce}\right]\Delta f$$

Fig 5—A simplified bipolar transistor noise model using white-noise sources.

oscillation. The circuit's amplitude stabilization mechanism is responsible for sustaining oscillation. We can view the oscillator as a two-terminal negative-resistance generator, as shown in Fig 3. Here, the total resistance—the sum of the resonator resistance and the resistance of the two-terminal oscillator—must be less than or equal to zero for oscillation. The net reactance will be zero at resonance. A different view is presented in Fig 4, where the oscillator is treated as a feed-forward amplifier with positive feedback. We analyze this model by finding the gain (or loss) and the phase shift of both the amplifier and the feedback network. The product of the amplifier and feedback network gains must be greater than 1, and the total phase shift should be 360° or some multiple thereof.

Although we can't precisely analyze the large-signal operation of a circuit using wholly linear techniques, we should recognize some effects that will impact our linear analysis. Chief among these is bias shift. The large signals present in the circuit in a bipolar oscillator will cause a shift in the bias current, because of the nonlinearity of the base-emitter junction. The device current may be about 10% different from the nominal (no-signal) current and may shift in either direction (more current or less). Since the flicker-noise is bias dependent, this effect is important to keep in mind.

The recommended approach to finding the bias-dependent loading of the resonator by the active device is to construct a linearized model of the device using its measured S-parameters at a particular bias point. This is especially important at higher frequencies. For simplicity, we have chosen not to do this in the example that follows, but to use a simple model.

Over a wide range of current, the device f_t remains constant. Since:

$$f_t = \frac{1}{2\pi R_d C_e}$$

where R_d is the emitter diffusion resistance and C_e is the emitter capacitance, and since:

$$R_d = \frac{26\ \text{mV}}{I_E}$$

(at room temperature), where I_E is the emitter bias current, we can therefore adjust the R_d and C_e parameters of our device model to reflect the bias current we expect to use. This will allow our linear circuit model to reflect the bias dependency of the oscillator.

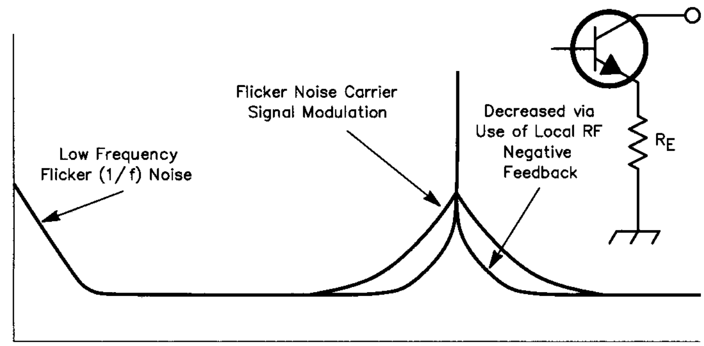


Fig 6—Adding negative feedback can reduce the amount of AM-to-PM modulation of the carrier by the transistor's flicker noise.

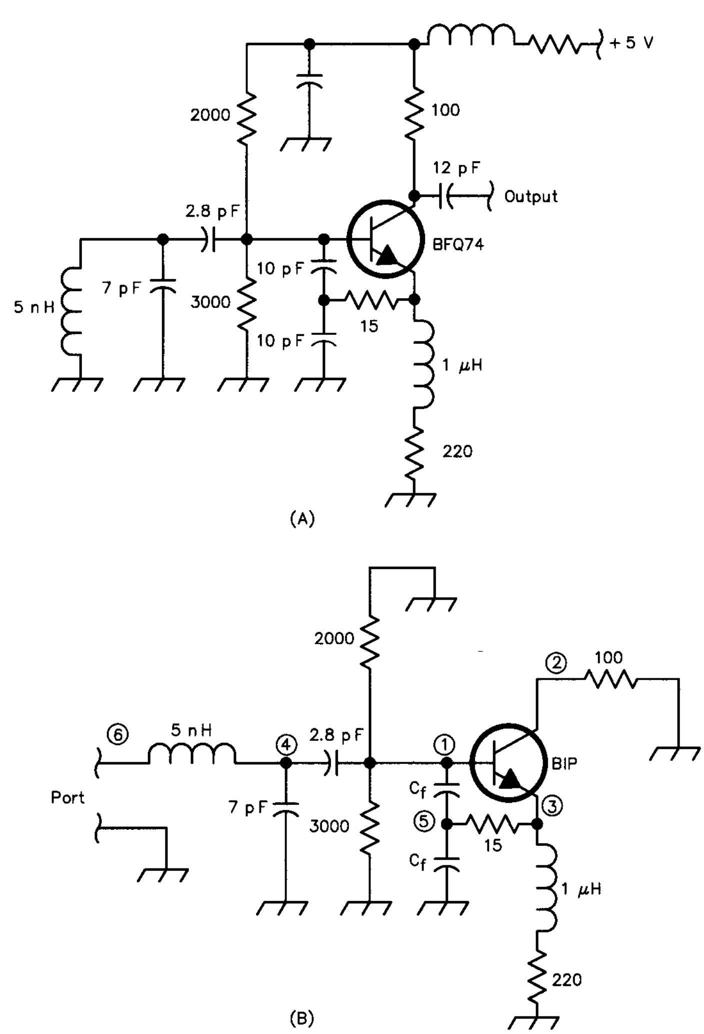


Fig 7—A simple 800-MHz oscillator circuit. The schematic is shown at A, and the circuit model for simulation is shown at B. The circuit model treats the circuit as a 1-port device, in order to investigate the impedance at the resonator.

As mentioned before, flicker noise is dependent largely on the bias current. But the *effect* of flicker noise can be reduced. This noise contributes to the phase noise by modulating the oscillator's frequency via AM-to-PM conversion. We can reduce this modulation by use of negative feedback. A simplified noise model of a transistor is shown in Fig 5. The effect of applying negative feedback to reduce phase noise is shown in Fig 6.

Linear Analysis by Simulation

By far, the easiest way to perform the linear analysis to optimize an oscillator circuit is via linear circuit simulation. Simulators such as *ARRL Radio Designer* (a subset of Compact Software's *Super-Compact* linear simulator) can provide a look into the oscillator circuit, allowing us to adjust circuit parameters to achieve the optimal circuit for the devices being used.[4]

A simple oscillator circuit is shown in Fig 7. This 800-MHz oscillator uses a Siemens BFQ74 bipolar transistor. Looking at this circuit from the standpoint of the negative-resistance generator of Fig 3, we analyze the net resistance of the resonator (L1) and the oscillator circuit. The resistance should be 0 or slightly negative.[5] We most easily view this by breaking the circuit at the ground connection of the coil and treating that point and ground as the terminals of a 1-port circuit, so we can investigate its impedance. The circuit model is shown in Fig 7B.

We want to select a bias current that is as small as possible, without reducing it to the point where the oscillator output power is too small to give a useful ultimate signal-to-noise ratio. In this case, we selected a bias emitter current of 10 mA. Now we have to find the appropriate feedback network, consisting of C1 and C2. Varying these capacitance values will vary the feedback and thus the loading of the resonator by the oscillator circuit. Finding the point at which the net resistance of the modeled circuit is just negative gives us the proper feedback; at this point the loading is the least that will sustain oscillation, and the loaded Q is therefore the highest available with the selected bias.

Fig 8 shows the circuit netlist used with *ARRL Radio Designer* to simulate the circuit of Fig 7B, and Fig 9 shows the port resistance (RZ11) and reactance (IZ11) calculated by the simulation. The traces labeled 1 are for values of C1 and C2 of 5 pF. Traces 2 are with C1 and C2 at 10 pF, and traces 3 are at 25 pF. What we are looking for here is the resistance at resonance, where the reactance is zero. For trace 3, this occurs at about 735 MHz. Here, the resistance is almost exactly zero. This allows no room for component tolerances or for adjusting the frequency upward, either of which may inhibit oscillation. Trace 2 shows a better result. At resonance, about 760 MHz, the resistance is negative, and it stays negative up through above 1 GHz. Small variations in component values, or adjusting the frequency upward, should not keep the circuit from oscillating. Trace 1 might seem to be even better because the resistance is more negative, but now we are loading the resonator—and lowering the loaded Q—more than we need to. This is shown in Fig 10, which shows the magnitude of the impedance for the same three cases.

Even though the resistive part of the impedance is negative, we can use the magnitude of the impedance to determine the loaded Q. From Fig 10 we can find the impedance at resonance, then find the 3-dB points on the curve, by multiplying the resonant impedance by 1.414. The loaded Q is then the resonance frequency divided by the 3-dB bandwidth. (This is more easily found by outputting the data of Fig 10 in tabular form.) It's obvious from the graph that the Q of trace 1 is lower than that of trace 2. For low phase noise, therefore, trace 2 is a better choice. Setting C1 and C2 to 10 pF results in certain oscillation and good phase noise.

Finally, the linear approach can be extended to further optimize the circuit. The L/C ratio of the resonator could be reduced, reducing coupling and increasing the loaded Q. If we had an ideal FET, we could theoretically achieve the performance predicted by the Leeson model and graphed in Fig 11.[6]

VCO Noise

So far, we've considered only the noise from the transistor. When we extend our design to become a VCO, by adding a tuning diode, we must also consider the phase noise introduced by that diode. Contrary to what you may have read elsewhere, this noise is not due solely to Q reduction from the added diode. The diode itself introduces noise that modulates the VCO frequency. The easiest way to analyze

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*
*  ARRL Radio Designer 1.0
*  COMPACT SOFTWARE, Inc.
*  Copyright (C) 1988-1994. All Rights Reserved.
*
*  SIEMENS BFQ 74 BPT: Analysis of an NPN bipolar model.
*  bias network is set for Ie=10mA
*****************************************************
Cf:10pF          ; Tapped-capacitor feedback network
IE:10mA          ; Emitter current
FT:6000e6        ; Device ft in Hz
Rd:(26mV/IE)
Cte:(1/(2*PI*FT*Rd))
*****************************************************
BLK
   BIP 1 2 3 A=0.98 RB1=4 CE=Cte RE=Rd
* Feedback network
   CAP 1  11 C=Cf
   CAP 11 0  C=Cf
   RES 3  11 R=15
* Emitter feedback network
   SRL 3  0  R=220 L=1UH
* Tank circuit
   CAP 1  4  C=2.8PF
   IND 4  31 L=5NH F=800MHZ Q1=120
   CAP 4  0  C=7PF
* Collector decoupling
*    CAP 2  0  C=1NF
     RES 2  0  R=100
* DC bias network
   RES 1  0  R=2000
   RES 1  0  R=3000
   OSC  :1POR 31
END
*
*************************
* FREQ: Frequency block *
*************************
FREQ
  STEP 500MHZ 1000MHZ 10MHZ
  STEP 700MHz 850MHz 2MHz
END
*************************************
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Fig 8—An *ARRL Radio Designer* netlist that describes the circuit model of Fig 7B.

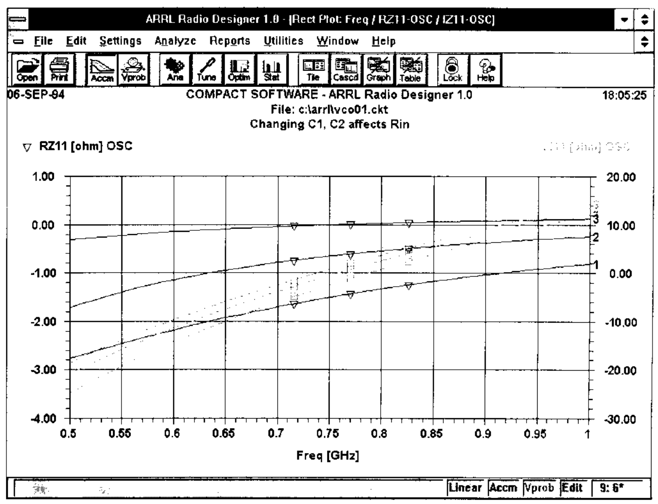

Fig 9—This *ARRL Radio Designer* analysis shows the resistive (RZ11) and reactive (IZ11) parts of the impedance seen at the port of Fig 7B. A negative resistance at resonance ensures oscillation. Trace 1 is with C1 and C2 at 5 pF, trace 2 has them at 10 pF and for trace 3 they are set to 25 pF.

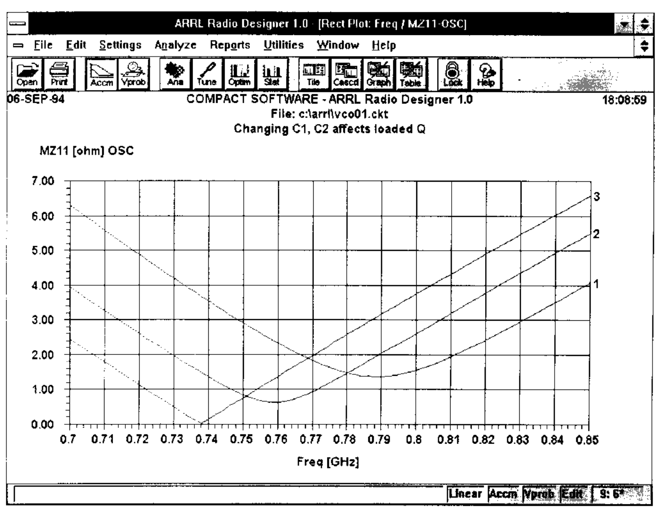

Fig 10—The magnitudes of the impedances plotted in Fig 9 are shown here. The reduction in Q as the feedback capacitors are decreased in value is dramatic.

this noise is to treat the diode's noise contribution as that of an equivalent resistance, R. This resistor can then be considered to be generating the thermal noise voltage that any resistance exhibits:

$$V_n = \sqrt{4KT_0R\Delta f} \qquad \text{Eq 1}$$

where V_n is the open-circuit RMS thermal noise voltage across the diode, K is Boltzmann's constant, T_0 is the temperature in Kelvins, R is the equivalent noise resistance of the tuning diode, and Δf is the bandwidth we wish to consider. At room temperature (about 300 K), KT_0 is 4.2×10^{-21}.

Practical values of R for tuning diodes range from about 1 kΩ to 50 kΩ. For a value of 10 kΩ, for example, we would find a noise voltage from Eq 1 of:

$$V_n = \sqrt{4\times 4.2\times 10^{-21}\times 10{,}000}$$
$$= 1.265\times 10^{-8}\ \ \mathrm{V}/\sqrt{\mathrm{Hz}}$$

This noise voltage from the tuning diode modulates the frequency of the oscillator in proportion to the oscillator's VCO gain, K_0, (the frequency swing per volt of the tuning signal):

$$(\Delta f_{\mathrm{rms}}) = K_0 \times (1.265\times 10^{-8}\,\mathrm{V}) \qquad \text{Eq 2}$$

in a 1-Hz bandwidth. This can be related to the peak phase deviation, θ_d:

$$\theta_d = \frac{K_0\sqrt{2}}{f_m}(1.265\times 10^{-8}\,\mathrm{rad}) \qquad \text{Eq 3}$$

in a 1-Hz bandwidth, where f_m is the frequency offset of the noise from the oscillator operating frequency. Applying a typical VCO gain of 100 kHz/V gives a typical peak phase deviation of:

$$\theta_d = \frac{0.00179}{f_m}\,\mathrm{rad} \qquad \text{Eq 4}$$

in a 1-Hz bandwidth. For an offset of 25 kHz, as might be used to find the noise in an adjacent FM channel, this gives $\theta_d=7.17\times10^{-8}$ rad in a 1-Hz bandwidth. Finally, we can convert this result into the SSB signal-to-noise ratio at the specified frequency offset:

$$L(f_m) = 20\log_{10}\frac{\theta_d}{2} = -149\,\mathrm{dB/Hz} \qquad \text{Eq 5}$$

This kind of noise performance is typical of a high-end laboratory signal generator such as a Rohde and Schwarz SMGU or a Hewlett-Packard 8640. It's interesting to note that the resonators used by these two products are slightly different. The SMGU uses a helical resonator while the 8640 uses an electrically shortened quarter-wave cavity. Both generators are mechanically pretuned, allowing use of a relatively small electrical tuning range, at about 100 kHz/V, for FM and AFC purposes. It's worth noting, too,

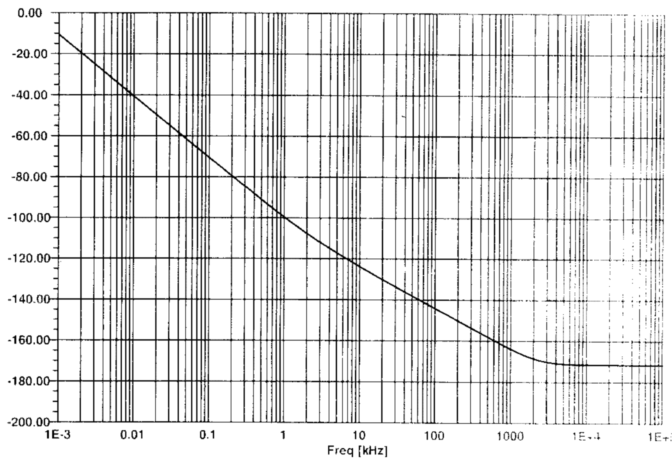

Fig 11—The Leeson equation, plotted for an ideal FET, showing phase noise in dBc/Hz versus frequency offset from the carrier. Note that the flicker-noise corner frequency is apparent at about 1 kHz.

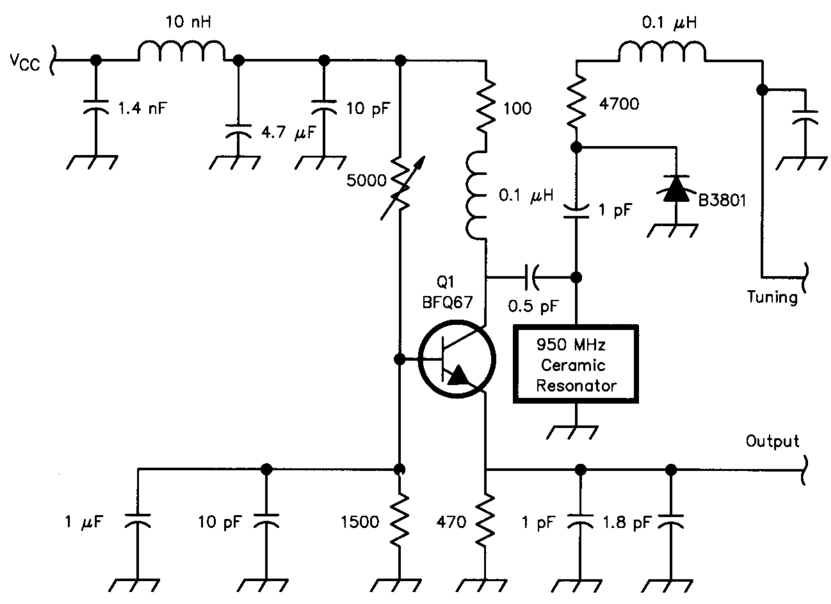

Fig 12—An example 800-MHz VCO circuit.

that the nonlinear capacitance-vs-voltage characteristic of a tuning diode results in a tuning sensitivity—and thus a noise performance—that depends on the input tuning voltage.

Fig 12 shows a typical VCO circuit. The measured phase noise of this oscillator is shown in Fig 13. While we cannot directly predict the phase noise of a circuit using only linear simulation (we will see such a prediction when we discuss the nonlinear approach), following the techniques described above can help us optimize the circuit. And we can also trade off the modulation sensitivity against the resulting phase noise, using Eqs 1, 3 and 5. This trade-off is shown in Fig 14, which graphs phase noise versus modulation sensitivity for the VCO.

Improving VCO Performance

We can improve the noise performance of a VCO by using multiple tuning diodes in the antiparallel arrangement of Fig 15. The improvement arises from two causes. First, the individual parallel diodes each have a smaller capacitance value than a single diode would need. This helps because small-capacitance diodes have less noise (lower equivalent noise resistances) than larger-capacitance diodes, due to the fabrication technology. Second, because the noise voltages from the individual diodes are uncorrelated, they do not directly sum together. Thus the effective noise is less than that of a single diode. While this scheme increases the cost of the circuit, it can reduce the diode noise contribution by as much as 15 or 20 dB compared to using a single diode. The result can approach the performance of a resonator using a single high-Q capacitor.

The Nonlinear Approach

Nonlinear circuit simulation allows us to fully predict oscillator circuit performance, including noise. In this case, we rely on a large-signal model for the transistor, such as the Curtice, Statz, TOM or Materka FET models, or the Gummel-Poon bipolar transistor model. To use this approach successfully requires careful parameterization of the device.

A nonlinear simulator such as Compact Software's *Microwave Harmonica* can generate the exact output power, bias-dependent Q and noise performance of the oscillator, using an harmonic-balance technique. In Compact's *Microwave Harmonica* and *Scope* products, a frequency-dependent color-noise transistor model is used in addition to the calculation of flicker noise. Higher-frequency transistor

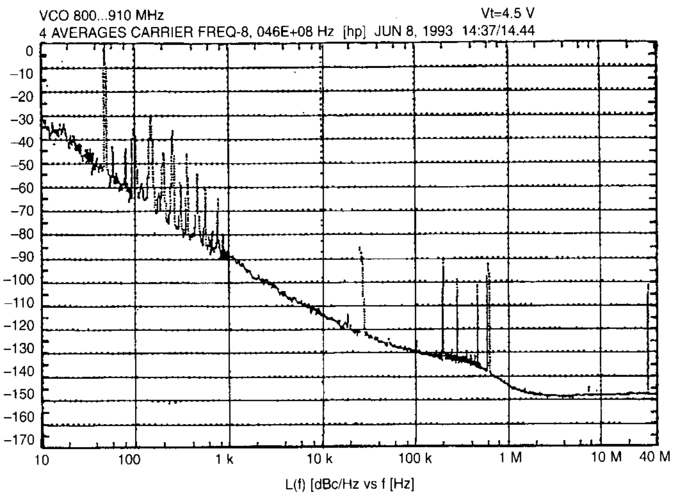

Fig 13—Measured phase noise of the oscillator of Fig 12.

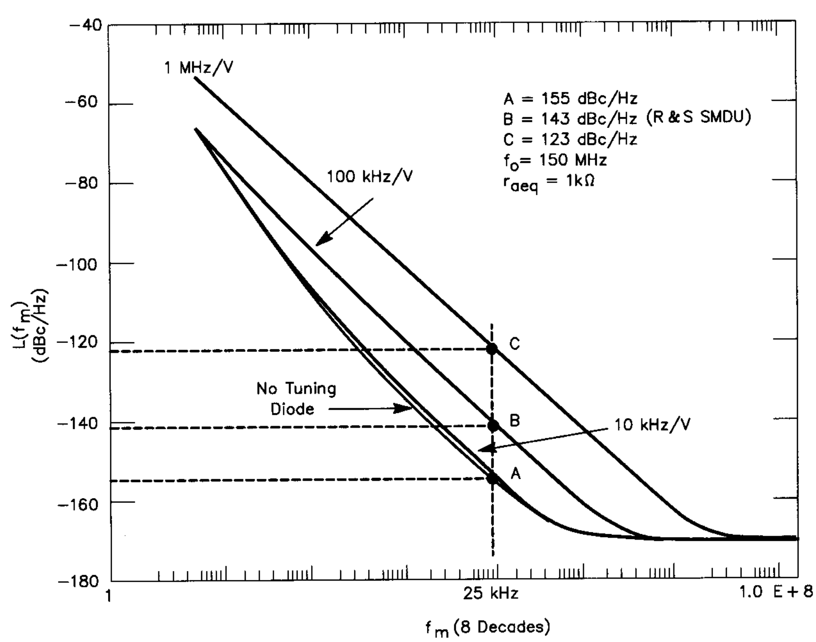

Fig 14—Phase noise increases as the tuning sensitivity of the VCO is increased, as shown here. r_{aeq} is the equivalent noise resistance of the tuning diode.

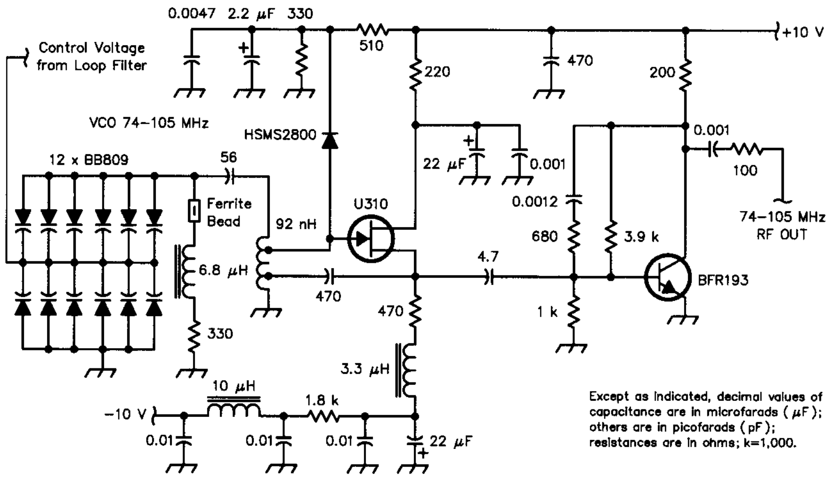

Fig 15—Improved phase-noise performance can be obtained by using a number of tuning diodes in the antiparallel arrangement shown here. The 92 nH coil is a 4-turn coil tapped at 1 and 2 turns from the ground end.

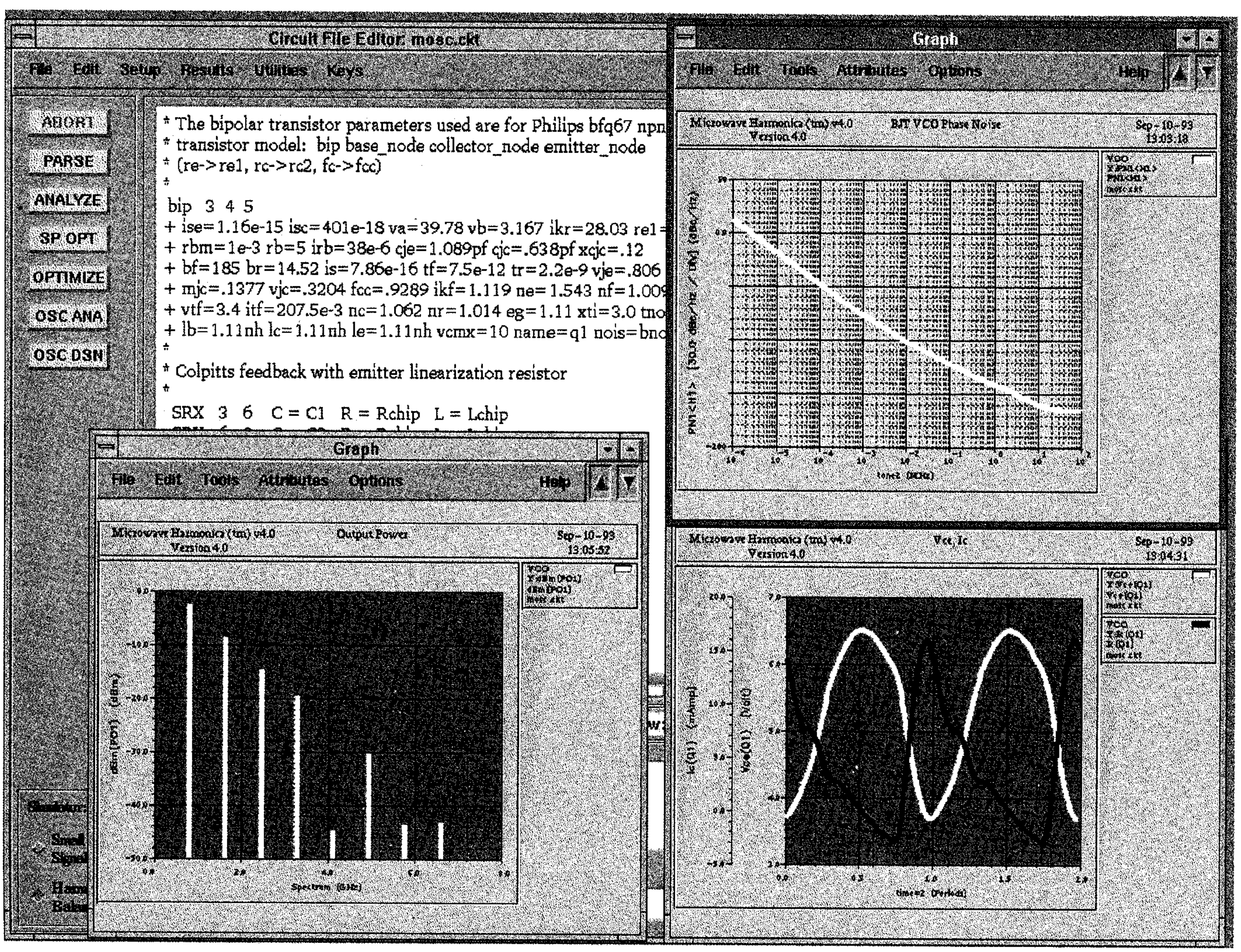

Fig 16—A *Microwave Harmonica* nonlinear analysis shows the output power spectrum, waveform distortion and phase noise of the oscillator of Fig 12.

noise is also taken into account.[7,8,9,10,11]

Fig 16 shows a *Microwave Harmonica* analysis of a Motorola 800-MHz VCO circuit similar to that of Fig 7. Included in the simulation is the noise contribution of the tuning diode.

We also can use nonlinear analysis to investigate the effect of adding a gate-clamping diode to a JFET oscillator, which is often seen in published circuits such as that of Fig 17. Figs 18 and 19 show the results of such an analysis, which shows that the clamping diode seriously degrades the noise performance of the oscillator.[12,13,14]

Coaxial Ceramic Resonators

None of the techniques we've described here can make up for a poor unloaded Q of the resonator in an oscillator circuit. But to get both small size and a high Q can be difficult. At UHF and above, one solution is the use of ceramic resonators. Siemens and other companies offer silver-plated ceramic quarter-wave TEM-mode resonators for operation at 400 to 4500 MHz. Mechanically rugged and small, these are ideal resonators for oscillators and filters in portable equipment.

These devices are shorted coaxial quarter-wave lines with silver plating on the conducting surfaces. The dielectric is one of three different relative permittivities (ε_r) of 21, 38 or 88. The needed length of a resonator can be found from:

$$L = \frac{\lambda}{4\sqrt{\varepsilon_r}} \qquad \text{Eq 6}$$

Table 2 shows typical ceramic resonator types. Larger-diameter (and higher Q) resonators can be made at customer request. Designing with these resonators is fairly simple despite the complicated procedures published elsewhere.[15]

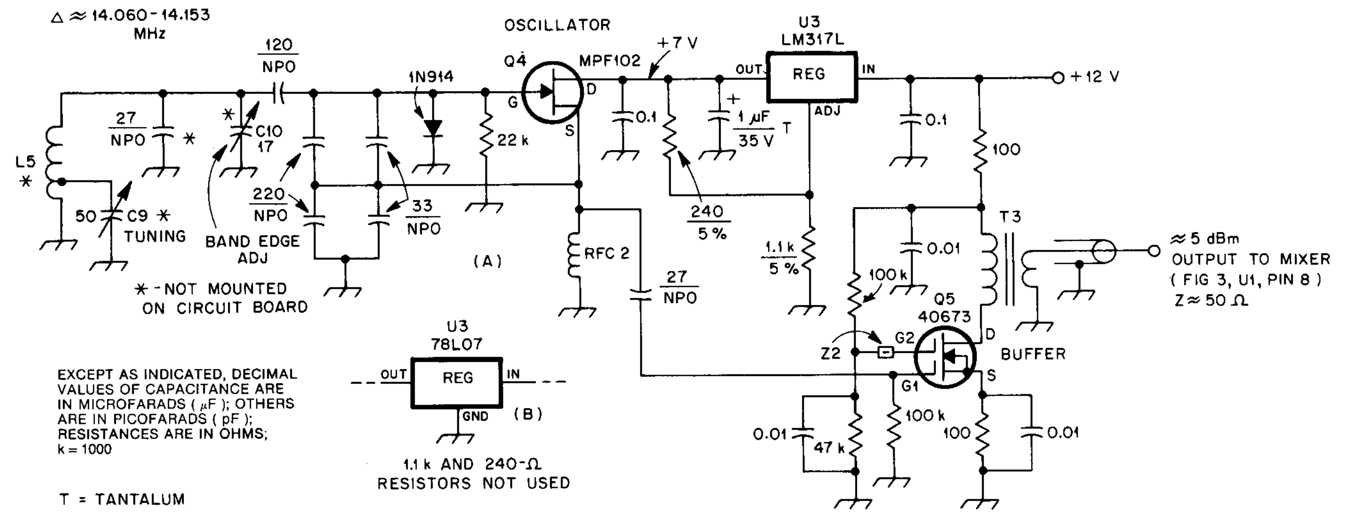

Fig 17—An oscillator with a gate clamping diode added. Predicted phase noise of the circuit is shown in Figs 18 and 19. Confirming phase-noise measurements were made at 10 MHz, after adjusting L5 for operation at that frequency.

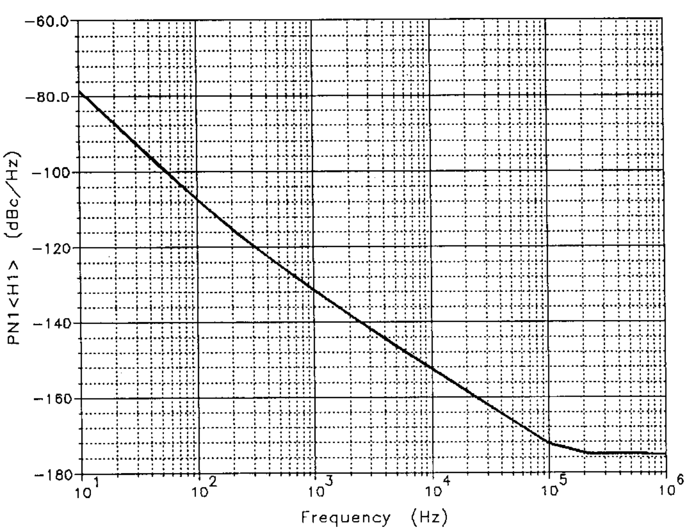

Fig 18—The phase noise of the oscillator of Fig 17.

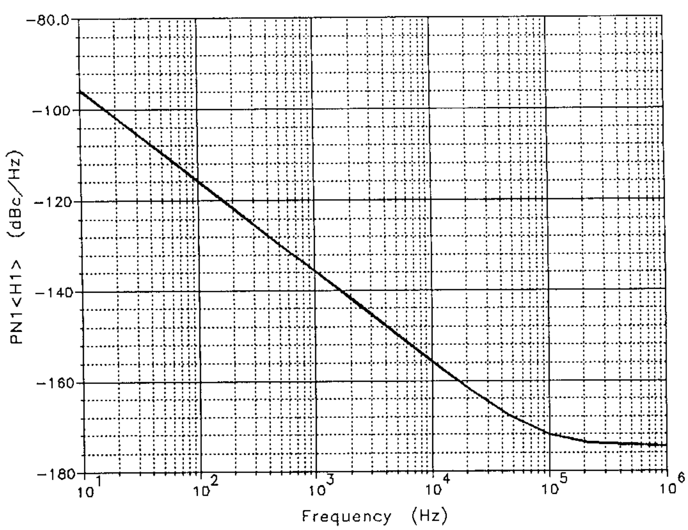

Fig 19—Without the gate clamping diode, the circuit of Fig 17 shows remarkably improved phase noise. Contrast this graph with that of Fig 18.

Equivalent Circuit Computation

Let's assume we want to design an oscillator for 900 MHz. The first thing we need to do is assume that because of loading effects we need to set the ceramic resonator frequency about 10% higher than the operating frequency. The characteristic impedance, Z_0, of a round coaxial resonator is about:

$$Z_0 = \frac{Z}{\sqrt{\varepsilon_r}} \ln(D/d) \quad \text{Eq 7}$$

the value of Z depends on the shape of the resonator. For round resonators, Z is about 76.5 Ω. We'll use a resonator with ε_r=38, D=6.0 mm and d=2.5 mm. This gives a Z_0 of:

$$Z_0 = \frac{76.5}{\sqrt{38}} \ln(6.0/2.5) = 10.8 \ \Omega$$

or about 11 Ω. Using the fact that:

$$Z_0 = \sqrt{\frac{L}{C}} \quad \text{Eq 8}$$

we can solve for L:

$$L = Z_0^2 C \quad \text{Eq 9}$$

and plug this into the formula for resonant frequency:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \text{Eq 10}$$

Finally, we can solve for C:

$$C = \frac{1}{2\pi f Z_0} \quad \text{Eq 11}$$

Performing these calculations for our example 990-MHz resonator gives a capacitance of about 14.7 pF and an inductance of 1.18 nH. With an unloaded Q of about 500 to 600, the parallel equivalent resistor is about 6000 Ω. The approximate length of the resonator, from Table 2, is 12.6/f mm. We now have all the needed information.

We can use the calculated L, C and R values to model the circuit. Even better, though, would be to model the resonator as a transmission line.

With the addition of an external capacitor at the open end of the resonator, the frequency can be reduced about 20%. A tuning range of about 5% is also possible. Fine tuning can be performed using a varactor diode, such as a high-Q, linear-frequency diode from Siemens. Some suggested bipolar transistors for use at 900-MHz are Siemens BFQ92P, BFS17, BFR35A and BFQ81.

To achieve good performance, the ceramic resonator should be mounted horizontally and soldered to the PC board ground on both sides along its entire length. When this is done, the resonator is wholly shielded, making it insensitive to stray fields and reactances.

Table 2—Typical Ceramic Resonator Characteristics

	ε_r=21	ε_r=38	ε_r=88
Material	$(MgCa)TiO_3$	$(ZrSn)TiO_4$	$(BaPb)NdO_3$
Permittivity	21 ± 2	38 ± 2	88 ± 5
D (mm)	5.5 ± 0.1	6.0 ± 0.1	5.7 ± 0.1
d (mm)	2.2 ± 0.1	2.5 ± 0.1	2.3 ± 0.1
L (mm)	$16.6/f_{res}$	$12.6/f_{res}$	$8.2/f_{res}$
Typical Q	800	500	300
Freq range (MHz)	2500-4500	800-2500	400-1600

Notes

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